

E-BEAM VOLTAGE POTENTIAL CIRCUIT PERFORMANCE LIBRARY

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TECHNICAL FIELD

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The present invention is directed to a cell library of image contrast values that can be correlated to and generated from a layout database.

DESCRIPTION OF THE DRAWINGS

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Fig. 1 shows a schematic representation of an SEM inspection apparatus that can be utilized in generating integrated circuit image contrast values in accordance with the concepts of the present invention.

Fig. 2A provides an image of an example net cell.

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Fig. 2B provides a voltage contrast image of the Fig. 2A net cell, generated in accordance with the concepts of the present invention, for a malfunctioning circuit.

Fig. 2C provides a voltage contrast image of the Fig. 2A net cell, generated in accordance with the concepts of the present invention, for a functioning circuit.

25 Figs. 3A-3F are a collection of SEM micrographs showing an anomalous cite detected in accordance with the concepts of the present invention.

Fig. 4 is a flow chart showing an overview characterizing, calibrating and library building of voltage contrast values for circuit cell structures in accordance with the concepts of the present invention.

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DESCRIPTION OF THE INVENTION

The present invention utilizes a point-by-point image contrast value generated from secondary electron collection during unbiased electron or ion beam bombardment of an integrated circuit (IC) under analysis in a vacuum environment to quantify the physical and electrical integrity of connections within the individual circuit cells of the IC device. This information can be stored for each type of circuit cell under standardized conditions to quantify and check the performance of individual circuit cells on the device. Circuit cell libraries of these values can be created, stored and used as standards for the debug of new products. The values can eventually be automatically generated and a routine option associated with the circuit layout database file can be used as necessary. The generated image file can then be utilized as a reference to show what the circuit cell voltage contrast should be when compared to the actual circuit cell voltage contrast data image of a device under debug analysis once the design has been transferred onto silicon. This verification method can be used for faster debug of new designs and requires less design engineering time for the analysis.

As shown in Fig. 1, the IC sample under analysis 10 is placed on a grounded substrate mount 12 with circuitry facing up. It is then placed on an x,y stage 13 in a vacuum chamber 14 with an electron or ion bombardment source 16 and a secondary electron detector system 18, such as a scanning electron microscope, a focused ion beam system, or an e-beam probe system. The IC 10 is not biased with external power. Analysis conditions, such as bombardment energy, are standardized to optimize the image contrast for different processing technologies. Contrast images can be collected at all levels of circuit processing such as at poly, contact, metal1 (M1), dielectric1 (D1), metal2 (M2), etc.

As a beam 19 from the electron/ion bombardment source 16 rasters across surface of the integrated circuit (IC) 10 during SEM (Scanning Electron Microscopy) inspection as shown in Fig. 1, secondary electron reflection 20 dictates the brightness level of the acquired images. Sites with more reflected electrons as a result of higher secondary yield would appear brighter, whereas sites with electron returning paths would appear darker due to less secondary electrons available to the detector system 18. As a result, under static or an

equilibrium condition, the level of brightness relates to the electron culmination and, therefore, to potential level at the site.

Grayscale levels typically used in image capturing systems can quantify the level of brightness. An 8-bit system will have 256 levels of grayscale. In our application, we used the difference in grayscale level to identify faulty circuitry physically. As illustrated in Figs. 2B and 2C, inspection and comparison of the same circuitry (Fig. 2A) between a “good” IC (Fig. 2B) and a bad IC (Fig. 2C) revealed differences in voltage contrast at the arrows. In this case, the reference image (Fig. 2A) is taken from another known good device at the same location under the same SEM inspection conditions.

Figs. 3A-3F are collections of SEM micrographs showing an anomalous site. In this application, because of the regularity of the IC structures, any of the repeated array elements can be used as a reference.

Figs. 3A and 3B are examples taken at the M@ level showing the value of a contrast image library. In Fig. 3A, the anomalous site appears brighter than the references. Fig. 3B shows a close-up view of the contrast difference. Similar contrast comparisons are shown at various de-processing steps from Figs. 3A through 3F. Fig. 3C is an example at the Via1 level of the process. Fig. 3D is an example at the metal1 (M1) level of the process. Fig. 3E is an example at the poly level of the process. Fig. 3F is an example at the composite level of the process.

It is apparent from the above that referencing to voltage contrast levels of pre-characterized to known reference structures provides quick and effective localization of anomalies. As an illustration, the 8-bit grayscale levels at the anomalous and reference sites in SEM micrographs Figs. 3B through 3F are shown in Table 1. The digitization of grayscale levels enables comparison in automated operation.

TABLE 1

<u>Figure</u>	<u>Brightness at anomaly</u>	<u>Reference Brightness</u>
3B	254	120
3C at arrow	248	80
3D shorted/reference poly	188	75
3E at arrow 1	254	157
3E at narrow 2	118	99

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The Fig. 4 flow chart provides an overview of the method of characterizing, calibrating and library building of the associated voltage contrast values at appropriate cell structures. It also illustrates the application of actual device analysis, during which a device layout database is coupled for navigation. The stored contrast values can be retrieved during SEM analysis to check for discrepancy.

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Although only specific embodiments of the present invention are shown and described herein, the invention is not to be limited by these embodiments. Rather, the scope of the invention is to be defined by these descriptions taken together with the attached claims and their equivalents.

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